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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/229,592	01/13/99	DOYLE B	42390.P5578

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EXAMINER	
BROCK II,P	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 06/08/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/229,592	DOYLE ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on th cover sheet with th corr spondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear if "etching the alignment component" in claims 10 and 11 is an additional step to "removing the alignment component" stated in claim 1, or an additional step. It is not clear how a removed alignment component from claim 1 could further be etched in claim 10 if it was actually removed.

Claim Rejections - 35 USC § 103

3. Claims 1 – 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder et al. (USPAT 6063677, Rodder) in view of Sekine et al. (USPAT 5937300, Sekine).

Rodder discloses a method of forming a transistor in figures 3a – 5.

In figure 3a Rodder disclose forming an alignment component (120 and 122) on a substrate (102) of a semiconductor material. Rodder discloses in figure 3b and column 3, lines 5 – 40 depositing a metal layer (106) over the substrate. Rodder discloses in column 3, lines 5 – 40 that the metal layer could also be a silicide layer. Rodder discloses in column 3, lines 15 – 16 that the silicide regions are self aligned to the disposable gate. It is an inherent feature of silicide regions that are self aligned to the disposable gate would extend up to the disposable gate and

have inner surfaces which face one another. In figures 3e and 3f Rodder discloses removing the alignment component. In figures 3e – 5 and column 5, lines 11 –26 Rodder discloses replacing the removed alignment component with a conductive gate (112) inherently substantially extending up to the silicide regions. Rodder does not disclose a method of forming the silicide regions. Sekine teaches in figure 13b depositing a metal layer (813) over a substrate (801) and an alignment component (805, 804 and 810). Sekine further teaches of reacting the metal layer with the semiconductor material of the substrate to form two silicide regions (814) that are self aligned to the alignment component, the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the method of forming silicide regions of Sekine that include lower and upper portions of silicide regions in the method of Rodder in order to decrease the resistance of the silicide film as stated by Sekine in column 2, lines 15 – 30. Because Rodder discloses in column 3, lines 15 – 16 that the raised source and drain regions are self aligned to the disposable gate it is further obvious that the silicide regions of the combined method of Rodder and Sekine would produce silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate.

With regard to claims 2 – 4, Rodder discloses in columns 2 and 3, lines 59 – 67 and 1- 4 respectively that the alignment component is made of silicon oxide which inherently posses the

properties of being non-conductive, and will not react with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

With regard to claims 5, 6 and 8, Rodder discloses in column 2, lines 11 – 17 that the alignment component is less than .10 microns wide. It is inherent that the alignment component has a thickness of between 1000Å and 2500Å. It is inherent that the metal layer is between 300Å and 400Å thick.

With regard to claim 7, Sekine discloses that the metal layer is titanium in column 2, lines 4 – 6.

With regard to claim 9, Sekine discloses in figure 13c that the silicide regions have lower surfaces located lower than a lower surface of the alignment component.

With regard to claim 10, Rodder discloses in figures 3c – 5 a method whereby the alignment component is replaced with the gate. In figure 3c Rodder discloses depositing a layer (114) over the silicide regions and the alignment component. In column 3, lines 46 – 49 Rodder discloses planarizing the layer at least until the alignment component is exposed. In figures 3e and 3f Rodder discloses etching the alignment component at least until the substrate is exposed to leave an opening between the inner surfaces of the silicide regions. In figures 3g – 5 Rodder discloses forming a gate (112) in the opening.

With regard to claim 11, it would be obvious in the method of Rodder in view of Sekine that after the etching of the alignment component, the upper portions of the inner surfaces would be exposed. Because the alignment component and the upper portions of the inner surfaces are in contact as applied to claim 1, when the alignment component is removed, the upper portions of the inner surfaces would be exposed.

With regard to claim 12, Rodder discloses in columns 2 and 3, lines 59 – 67 and 1 – 52 respectively the alignment component and the layer are made of different materials, one being made of silicon oxide and the other being made of silicon nitride.

With regard to claim 16, Rodder discloses in figure 4 forming doped regions (104) which extend from the silicide regions in underneath the gate.

4. Claims 13 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder and Sekine as applied to claim 1 above, and further in view of Inumiya et al. (USPAT 6054355, Inumiya).

With regard to claims 13, Rodder discloses in figure 5, and column 4, lines 56 – 67 depositing a gate dielectric layer (110), and forming a gate electrode on the gate dielectric layer. Rodder does not disclose forming a dielectric layer that would be sufficient in Rodder and Sekine because the dielectric layer of Rodder would not insulate the entire upper portion of the inner surface of the silicide regions of Rodder and Sekine. Inumiya teaches in figure 10g depositing a gate dielectric layer (116) lining the inside of a groove (114) formed by the removal of an alignment feature, and forming a gate electrode (117) on the gate dielectric layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the gate dielectric layer of Inumiya in the method of Rodder and Sekine in order to form a gate insulating film and a gate electrode in a groove formed by the removal of an alignment feature.

With regard to claim 14, it is inherent in the method of Rodder and Sekine in view of Inumiya that the gate dielectric could be less than 10Å thick.

With regard to claim 15, Rodder discloses that the gate electrode is made out of a metal in column 4, lines 64 – 67.

5. Claims 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder, Sekine and Inumiya as applied to claims 1 and 13 above, and further in view of Gardner et al. (USPAT 6051865, Gardner).

With regard to claims 17 and 18, Rodder, Sekine and Inumiya do not disclose using a high K dielectric layer. Gardner teaches in columns 3 and 4, lines 24 – 40 and 24-36 respectively a gate dielectric layer of barium strontium titanate that has a dielectric constant of at least 100. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the low K dielectric material of Gardner in the method of Rodder, Sekine and Inumiya in order to decrease the transistor threshold voltage as stated by Gardner in column 3, lines 26 – 33.

With regard to claim 19, Rodder, Sekine and Inumiya and Gardner does not disclose using platinum as a gate electrode. It is well known in the art to form a gate electrode of platinum. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the platinum gate electrode in the process of forming a transistor of Rodder, Sekine and Inumiya and Gardner in order to use a low-resistivity conductor for the gate material.

Response to Arguments

6. Applicant's arguments filed 4-24-2001 have been fully considered but they are not persuasive.

In response to the applicant's arguments "that Rodder does not disclose that the inner surfaces of the silicide regions contact the alignment component... that Sekine teaches this missing element in Fig. 13b with an alignment component composed of items 805, 804, 810, and silicide regions 814. These elements of Sekine fail to meet the limitations of claim 1 and therefore fail to teach the invention of claim 1." The only teaching gleaned from Sekine in the combination of Rodder and Sekine is a method to form silicide regions and to show the properties that a silicide formed in this way would exhibit.

Further, the figures of Rodder merely show one embodiment of the patented invention that are merely an artistic representation of an embodiment and not a factual real-life representation of what the invention of Rodder would look like if it were formed with silicide regions as suggested in the disclosure of Rodder as described above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yu discloses an alignment component consisting of a gate member and sidewall spacers which are all removed..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the

organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
June 7, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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